What is claimed is:

1. A semiconductor memory device, comprising:

a clock enable signal self refresh buffer for generating a self refresh clock enable signal by receiving the clock enable signal in the self refresh mode;

an internal clock signal generating unit for generating an internal clock signal by receiving the external clock signal;

a signal synchronization unit for generating an internal clock enable signal by synchronizing the clock enable signal with the internal clock signal;

a level detection unit for generating a level detection signal by detecting levels of the internal clock enable signal and the self refresh clock enable signal;

a clock self refresh buffer for receiving the external clock signal during a self refresh mode in response to the level detection signal; and

a self refresh command generation unit for activating a self refresh command in response to the level detection signal and inactivating the self refresh command in response to the level detection signal and an output signal of the clock self refresh buffer.

2. The semiconductor memory device as recited in claim 1, further comprising:

a clock normal buffer for receiving the external clock

signal in a normal mode; and

a clock enable signal normal buffer for receiving the clock enable signal in the normal mode.

3. A semiconductor memory device comprising:

a clock normal buffer for receiving an external clock signal in a normal mode;

a clock enable signal (CKE) normal buffer for receiving the CKE in the normal mode;

a CKE self refresh buffer for generating a self refresh clock enable signal by receiving the clock enable signal in the self refresh mode;

an internal clock generation unit for internal clock signal by receiving an output signal of the clock normal buffer;

a CKE clock synchronization unit for generating an internal clock enable signal by synchronizing the clock enable signal with the internal clock signal;

a CKE level detection unit for generating a CKE level detection signal by detecting levels of the internal clock enable signal and the self refresh clock enable signal;

a clock self refresh buffer for receiving the external clock signal during a self refresh mode in response to the CKE level detection signal; and

a self refresh command generation unit for activating a refresh command in response to the CKE level signal and inactivating the refresh command in response to the CKE level

signal and an output signal of the clock self refresh buffer.

4. The semiconductor memory device as recited in claim 3, wherein the clock self refresh buffer includes:

a signal generation unit for strobing the external clock signal;

a drive control unit for driving the signal generation unit when the self refresh command and the CKE-level detection signal are activated; and

an output control unit for outputting clock strobe signal by controlling an output signal of the signal generation unit in response to the self refresh command and the CKE level signal.

5. The semiconductor memory device as recited in claim 4, wherein the signal generation unit includes:

a signal edge detection unit for detecting an edge of the external clock signal under control of the drive control unit; and

a pulse width extension unit for outputting a first clock strobe signal by extending a pulse width of an output signal of the signal edge detection unit.

6. The semiconductor memory device as recited in claim 4, wherein the output control unit includes:

a NOR gate receiving an inverted self refresh command and the CKE level signal; and

a NAND gate for outputting a second strobe signal by receiving an output signal of the NOR gate and an output signal of the signal generation unit.

7. The semiconductor memory device as recited in claim 4, wherein the drive control unit includes:

an inverter for inverting the self refresh command; and

a NOR gate for generating a control signal to drive the signal generation unit by receiving an output signal of the inverter and the CKE level signal.

8. The semiconductor memory device as recited in claim 5, wherein the pulse width extension unit includes:

a delay unit for delaying an output signal of the signal edge detection unit;

a first NAND gate receiving an output signal of the delay unit and the output signal of the signal edge detection unit;

an inverter for inverting an output signal of the first NAND gate; and

a second NAND gate for generating the first clock strobe signal by receiving output signals of the inverter and the signal edge detection unit.

9. The semiconductor memory device as recited in claim 3, wherein the CKE clock synchronization unit includes:

an output signal strobe unit for strobing input signals;

an operation control unit for controlling an operation of

the output signal strobe unit in response to the clock strobe signal and the self refresh command;

an output signal generation unit for outputting the internal clock enable signal by receiving an output signal of the output signal strobe unit; and

an input signal generation unit for generating the input signals by receiving the output signal of the CKE normal buffer under control of the self refresh command and the self refresh clock enable signal.

10. The semiconductor memory device as recited in claim 9, wherein the operation control unit includes:

a first NAND gate receiving the self refresh command and the clock strobe signal; and

a second NAND gate for generating a control signal to control an operation of the output signal strobe unit by receiving an output signal of the first NAND gate and the internal clock signal.

11. The semiconductor memory device as recited in claim 9, wherein the input signal generation unit includes:

a first NAND gate receiving the self refresh command and the self refresh clock enable signal;

a second NAND gate output signals of the first NAND gate and the clock normal buffer;

a first inverter for outputting a first input signal by inverting an output signal of the second NAND gate; and

second and third inverters for outputting a second input signal by delaying the output signal of the second NAND gate.

12. The semiconductor memory device as recited in claim 11, wherein the output signal strobe unit for outputting the internal clock enable signal by receiving the first input signal under control of the operation control unit.

13. The semiconductor memory device as recited in claim 3, wherein the CKE level detection unit includes:

a set signal generation unit for generating a set signal by receiving an auto refresh signal and the internal clock enable signal; and

a signal generation unit for activating the CKE level signal in response to the set signal and inactivating the CKE level signal in response to the self refresh clock enable signal.

14. The semiconductor memory device as recited in claim 13, wherein the set signal generation unit:

a pulse width extension unit for extending a pulse width of the auto refresh signal;

a first NOR gate receiving the internal clock enable signal and a power up signal;

a second NOR gate for outputting a first set signal by receiving output signals of the pulse width extension unit and the first NOR gate and the self refresh clock enable signal;

and

a third NOR gate for outputting a second set signal by receiving self refresh clock enable signal and an inverted self refresh signal.

15. The semiconductor memory device as recited in claim 14, wherein the signal generation unit further includes:

a RS flip flop for activating an output signal of the RS flip flop in response to the first and second set signals and inactivating the output signal of the RS flip flop in response to the self refresh clock enable signal;

an initialization unit for initializing an output node of the RS flip flop in response to the power up signal; and

an inverter for outputting the CKE level signal by inverting an output signal of the RS flip flop.

16. The semiconductor memory device as recited in claim 3, wherein the self refresh command generation unit activates the self refresh command in response to activation of the CKE level signal and inactivates the self refresh command in response to the internal clock enable signal and the clock strobe signal.

17. The semiconductor memory device as recited in claim 16, wherein self refresh command generation unit includes:

a first NOR gate receiving the internal clock enable signal and the clock strobe signal;

a RS flip flop receiving an output signal of the first NOR gate and the power up signal as a reset signal and a CKE level signal as a set signal;

an initialization unit for initializing an output node of the RS flip flop; and

an output unit for outputting the self refresh command by inverting an output signal of the RS flip flop and a self refresh delay signal by delaying the self refresh command.

18. The semiconductor memory device as recited in claim 3, wherein the CKE clock synchronization unit includes:

an output signal strobe unit for strobing input signals;

a counting unit for counting the clock strobe signal in the self refresh period;

an operation control unit for controlling the output signal strobe unit in response to the clock strobe signal and the self refresh signal;

an output signal generation unit for generating the internal clock enable signal by receiving an output signal of the output signal strobe unit; and

an input signal generation unit for generating the input signals by receiving an output signal of the CKE normal buffer in response to an output signal of the counting unit and the self refresh clock enable signal.

19. The semiconductor memory device as recited in claim 18, wherein the counting unit includes:

a first shifting unit receiving an inverted clock strobe signal as a clock signal an inverted self refresh command as a reset signal and a self refresh clock enable signal as an input;

a first inverter for inverting the inverted clock strobe signal;

a first NAND gate receiving an output signal of the first inverter and the inverted CKE level signal;

a second shifting unit receiving an output signal of the first NAND gate as a clock signal, the inverted self refresh signal as a reset signal and an output signal of the first shifting unit as an input;

a second NAND gate receiving the output signal of the first inverter and the inverted CKE level signal; and

a third shifting unit receiving an output signal of the second NAND gate as a clock signal, the inverted self refresh signal as a reset signal and an output signal of the second shifting unit as an input.

20. The semiconductor memory device as recited in claim 19, wherein each of the shifting units includes:

a first transfer gate for transferring the input signal when the clock signal is inactivated;

a first latch for latching an output signal of the first transfer gate in response to the reset signal;

a second transfer gate for transferring an output signal when the clock signal is activated; and

a second latch for latching an output signal of the second transfer gate.

21. A self refresh method in a semiconductor memory device, comprising the steps of:

a) inactivating a clock enable signal and applying an auto refresh signal;

b) entering a self refresh mode in response to the clock enable signal synchronized with a clock signal;

c) receiving the clock enable signal in the self refresh mode;

d) activating the clock enable signal; and

e) exiting from the self refresh mode in response to the clock enable signal synchronized with the internal clock signal.

22. The self refresh method as recited in claim 21, wherein the step e) includes the steps of:

e1) activating a control signal synchronized with the clock signal in response to activation of the clock enable signal;

e2) detecting whether the clock enable signal is activated during activation of the control signal; and

e3) exiting from the self refresh mode according to a detection result.

23. A self refresh method in a semiconductor memory

device, comprising the steps of:

a) activating a clock enable signal and applying an auto refresh signal;

b) entering a self refresh mode in response to the clock enable signal synchronized with an internal clock signal;

c) receiving the clock enable signal in the self refresh mode;

d) updating a set value of a DLL circuit by receiving an external clock signal and activating the clock enable signal for a predetermined time referring to the clock signal in the self refresh mode;

e) exiting from the self refresh mode in response to the clock enable signal synchronized with the clock signal when the clock enable signal is activated over the predetermined time.